REMARKS

I. Status of the Application

Claims 21-40 are pending in this application. In the November 30, 2004 office action, the Examiner:

A. Objected to the drawings for certain issues relating to format;

B. Objected to claim 21-32 and 38-40 for informalities;

C. Rejected claims 33-34 under 35 U.S.C. § 102(e) as allegedly being anticipated by U.S. Patent No. 6,771,199 to Brooks et al. (hereinafter "Brooks");

D. Deemed claims 21-32 and 38-40 allowable if rewritten to overcome the noted informalities; and

E. Deemed claims 35-37 allowable if rewritten in independent format to incorporate all of the limitations of their respective base claim and intervening claims.

In this response, Figure 2 of the drawings has been amended as required by the Examiner. Applicants respectfully traverse the informality objections to claims 21-32 and 38-40, and respectfully traverse the prior art rejections of claims 33 and 34. Applicants request allowance of the application in view of the foregoing amendments and the following remarks.

II. The Objection to the Drawings is Moot

The Examiner objected to the drawings because Fig. 2 contained OR gates 2, 3 and 4 depicted in a manner that appeared similar to traditional AND gate symbols. Fig. 2 has been amended to show OR gates 2, 3, 4 depicted more traditionally. Applicant will supply formal

drawings upon approval of the correction. In light of the amendment to Fig. 2, it is respectfully submitted that the objection to the drawings is moot and should be withdrawn.

III. The Objection to the Claims

The Examiner objected to claims 21-32 and 38-40 due to alleged informalities. A first cited informality related to claims 21 and 38 reciting "a second number of multiplexers", and the second cited informality related to the claims referring to OR-gates while the figures allegedly showed AND-gates. (November 30, 2004 office action at p.2). Because of the above-discussed amendment to Fig. 2, it is submitted that the second cited informality relating to the OR gates in the claims is moot.

With respect to the first cited informality, the Examiner stated that

> independent claims 21 and 38 recite "a second number of multiplexer circuits" which misleading because there is no "first" number cited.

(*Id.*) Applicants respectfully traverse. Claims 21 and 38 both recite "a first number of OR gate circuits". In accordance with ordinary claim interpretation, the "first number" and the "second number" may be the same, but need not be.

Accordingly, one of ordinary skill in the art would readily determine that there is some "quantity" (first number) of OR gate circuits, and some "quantity" (second number) of multiplexer circuits, and that those numbers may or may not be the same. By contrast, if applicants had used "first number" to describe both the OR gate circuits and the multiplexer circuits, then it could be interpreted to mean that the number of OR gate circuits and the number of multiplexer circuits are identical.

It is therefore respectfully submitted that claims 21 and 38 are not misleading in reciting a "second number of multiplexer circuits", and that the objection to those claims should be withdrawn.

IV. The Anticipation Rejection of Claims 33 and 34 is in Error

In the November 30, 2004 office action, the Examiner alleged that claims 33 and 34 were anticipated by Brooks. For reasons discussed below in detail, it is respectfully submitted that Brooks fails to teach or disclose each and every element of the claimed invention. In particular, Brooks does not teach, among other things, a step of "performing an OR operation on bits of at least the m-1 more significant segments to generate at least m-1 output signals", as called for in claim 33 and 34. Brooks also fails to teach "summing the at least m-1 output signals" from the OR operation, as claimed.

A. Claim 33

Claim 33 is directed to a method for converting a binary input signal corresponding to a thermometer code into a binary output code. The method includes receiving an n-bit thermometer code and dividing the n-bit thermometer code into m segments. The method also includes performing an OR operation on bits of at least the m-1 more significant segments to generate at least m-1 output signals. The at least m-1 output signals are summed to produce a binary result that forms a first part of the binary output code. The method also includes multiplexing sets of bits of different segments, each set comprising bits having the same MSB significance within their respective segments, wherein the first part of the output code is used as multiplex selection signal. The multiplexed output signals add to produce, a binary result that

forms a second part of the binary output code.

B. Brooks Does Not Disclose an OR operation as claimed

Brooks does not disclose, among other things, performing an OR operation as claimed. The portions of Brooks cited against claim 33 include a code splitter and code shuffler of a mismatch shaping network 302.

In particular, with respect to the method steps of receiving and dividing an input thermometer code, the Examiner alleges that the digital signal input 304 of Brooks receives an n-bit thermometer code and that this code is divided up into segments illustrated as signals xeq0-xeq4. (Office action at p.3). With respect to the claimed method step of performing an OR operation on bits of the more significant segments, the Examiner further alleges that the shufflers 502a-502d of Brooks perform a logic operation on the signals xeq0-xeq4. The Examiner further appears to allege that the shufflers 502a-502d perform a summation of the results of the logic operation. (*Id.*)

Applicants respectfully submit that even if the Examiner has correctly characterized the teachings of Brooks, the Examiner has not set forth a prima facie case of anticipation. In particular, the Examiner alleges that Brooks teaches "performing a *logic* operation on bits of at least the m-1 more significant segments to generate at least m-1 output signals. . ." (*Id.*) (emphasis added). Even if true, this is *not* the same as "performing an *OR* operation on bits of at least the m-1 more significant segments to generate at least m-1 output signals". In other words, the disclosure of a "logic operation" does not constitute an anticipatory teaching of a claimed "OR operation". Accordingly, Brooks, as apparently admitted by the Examiner, *fails to teach performing and OR operation* as claimed.

Moreover, the shufflers 502a-502d do *not*, in fact, perform the claimed OR operation. While the shufflers 502a-502d of Brooks do have OR gates within them (see Fig. 6 of Brooks), the Examiner has not alleged, nor does it appear to be the case, that those OR gates receive perform OR operations on bits of m-1 more significant segments as claimed. Referring to Fig. 6 of Brooks, the OR gate 608 within the shuffler 502 does not receive the "bits of . . . the more significant segments". Instead, the OR gate 608 receives three values, each value being an ANDed result of a random sequence (from RAMs 606a-c) and another value xeq1', xeq2' and xeq3'. The values xeq1'-xeq3' are themselves derived from another ANDing of the *least significant* bits x<1> and x<0> with an enable signal. (See *id.*) As a consequence, the values that are ORed by the OR gate 608 of Brooks does not constitute bits of any segment of the input signal, much less bits of the more significant segments of the input signal.

Thus, to the extent the shuffler 502 of Brooks performs an OR operation, it does not perform "an OR operation on bits of at least the m-1 more significant segments", as claimed.

C. Brooks Does Not Teach Summing the Output of the OR Operation

Even if the bit shufflers did perform an OR operation as claimed, which they do not, Brooks also fails to teach a step of "summing the at least m-1 output signals", as claimed. In particular, as discussed above, the Examiner alleges that the shufflers 502a-502d of Brooks perform the step of "summing the output signals" of the "logic operation". (November 30, 2004 office action at p.3)

As discussed above, the only OR operation in the shuffler 502 of Brooks is the OR gate 608. The shuffler 502 contains no summation device connected to the output of the OR gate 608. In fact, the OR gate 608 is the final element of the shuffler 502 of Fig. 6 of Brooks. Thus,

the shuffler 502 does not perform any summing of the output of the OR gate 608, contrary to the Examiner's allegations.

As a consequence, Brooks fails to disclose the step of summing the output signals of the OR operation, as well as failing to disclose the OR operation itself.

D. Conclusion as to Claims 33 and 34

As discussed above, Brooks fails to disclose at least two different elements of claim 33, each of which is sufficient to establish patentability. It is therefore respectfully submitted that the anticipation rejection of claim 33 over Brooks is in error and should be withdrawn.

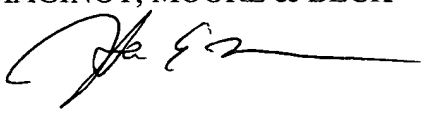
Claim 34 depends from and incorporates all of the limitations of claim 33. Accordingly, for at least the same reasons as those set forth above in connection with claim 33, it is respectfully submitted that the rejection of claims 34 over Brooks should be withdrawn.

V. Conclusion

For all of the foregoing reasons, it is respectfully submitted the applicants have made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully Submitted,

MAGINOT, MOORE & BECK



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Enclosures (replacement dwg)

Amendments to the Drawings

Please replace the drawing sheet 2/4 with the enclosed replacement page 2/4 with a proposed drawing change.